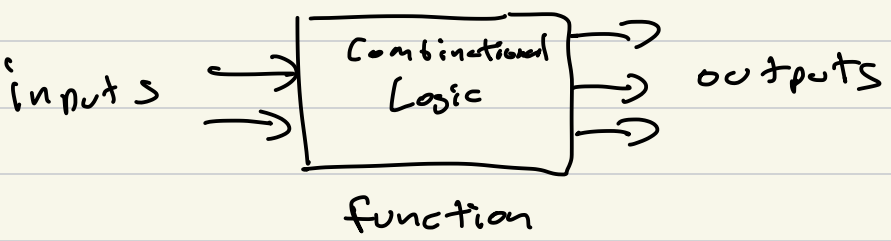
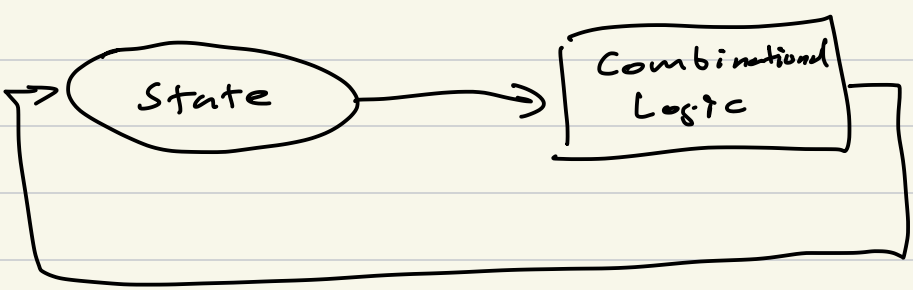
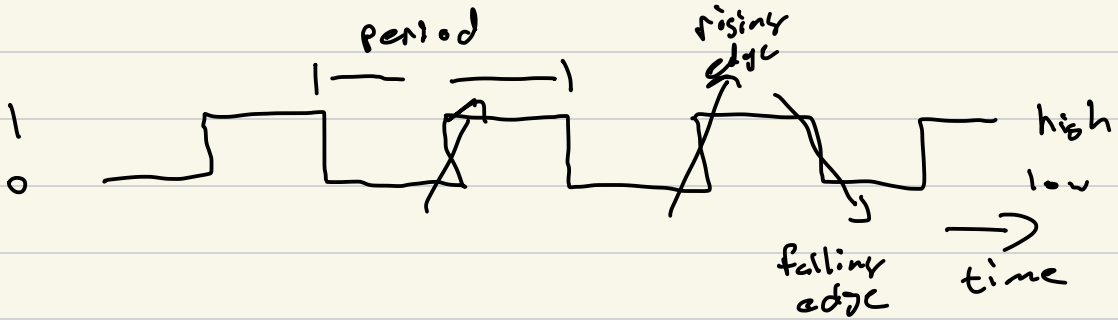
CS 315-01 Lab Sequential Logic Resisters





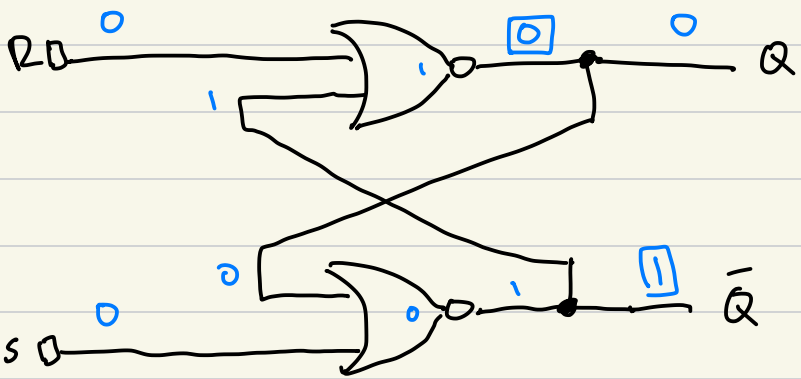
Clock cycle

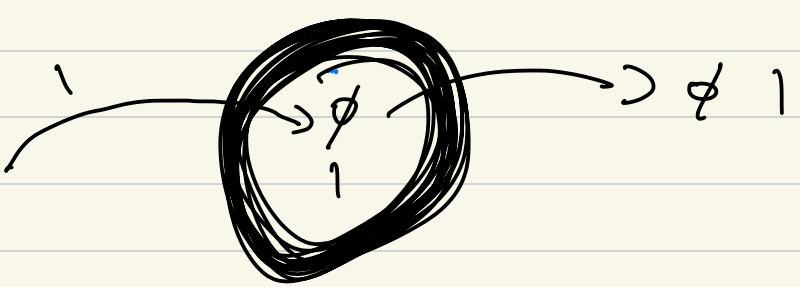


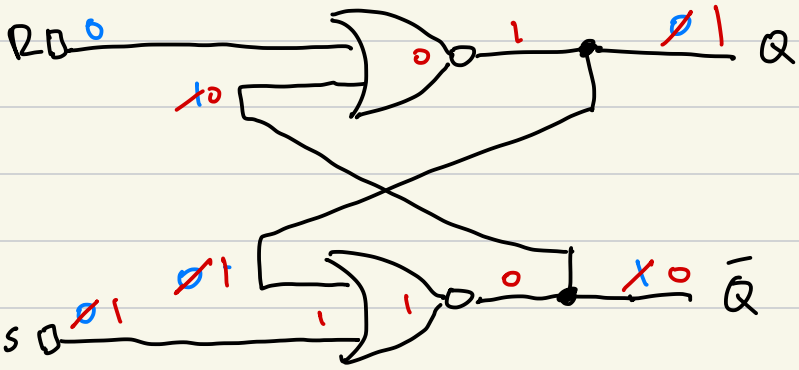
How to store a 1 bit value?

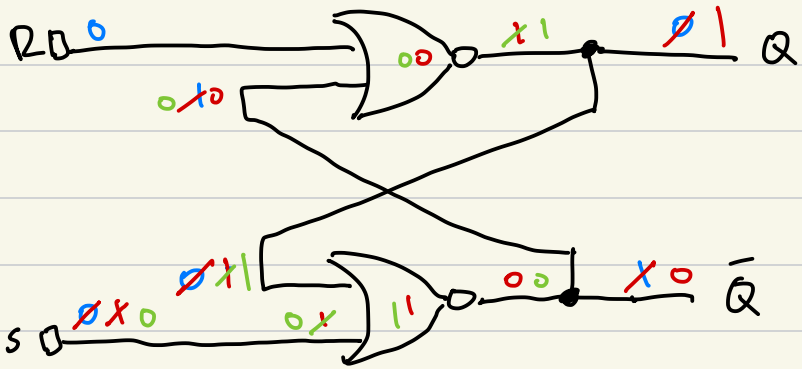
SR Latch set / reset

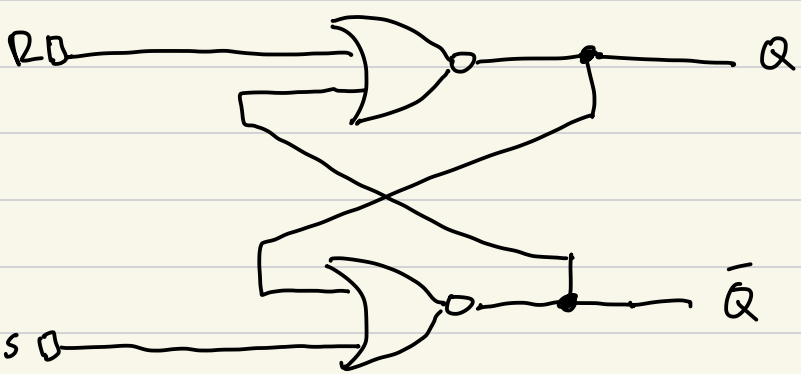
NOR gate






R
S
Q
$\bar{Q}$


R
S
Q
$\bar{Q}$


R
S
Q
$\bar{Q}$

time ↓

R	S	Q	$\bar{Q}$	
0	0	0	1	
0	1	1	0	
0	0	1	0	
1	0	0	1	
0	0	0	1	
1	1	X	X	undefined

SR Latch

D Latch (clock)

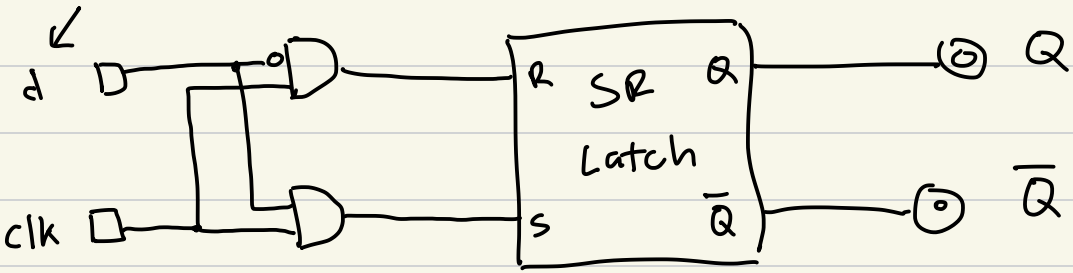
D Flip-Flop

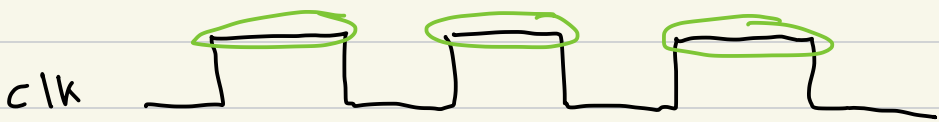
1 bit register

N bit register

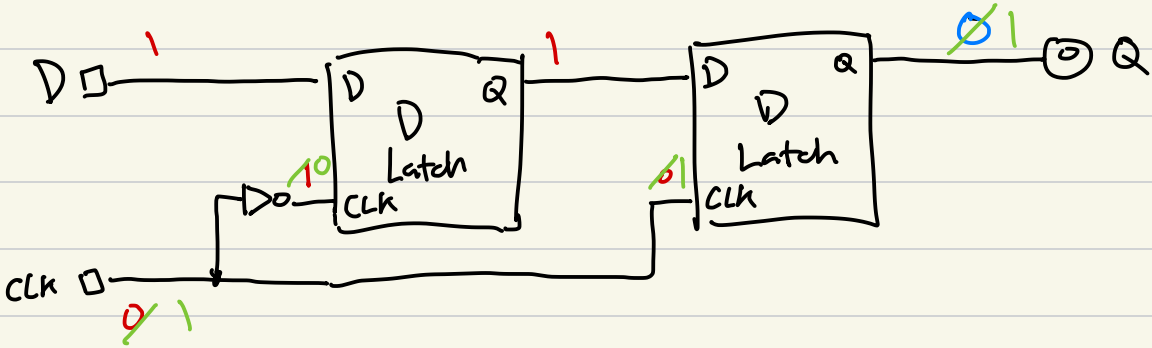
Counter

D Latch



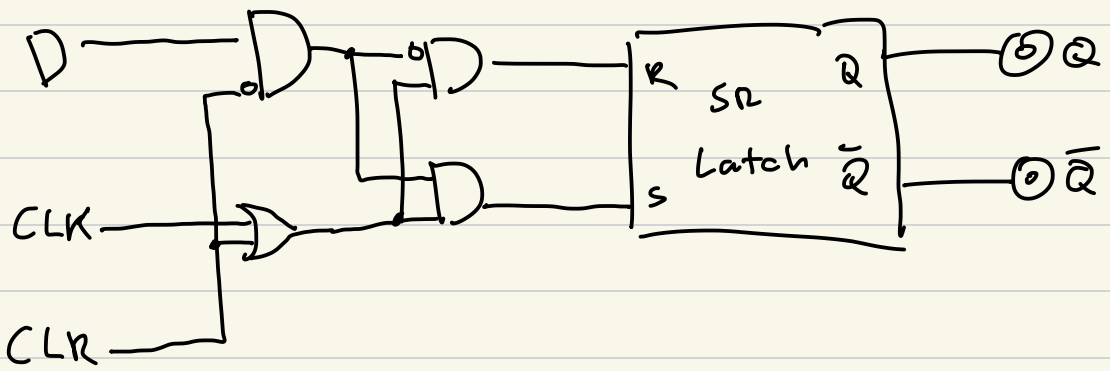


D Flip-flop

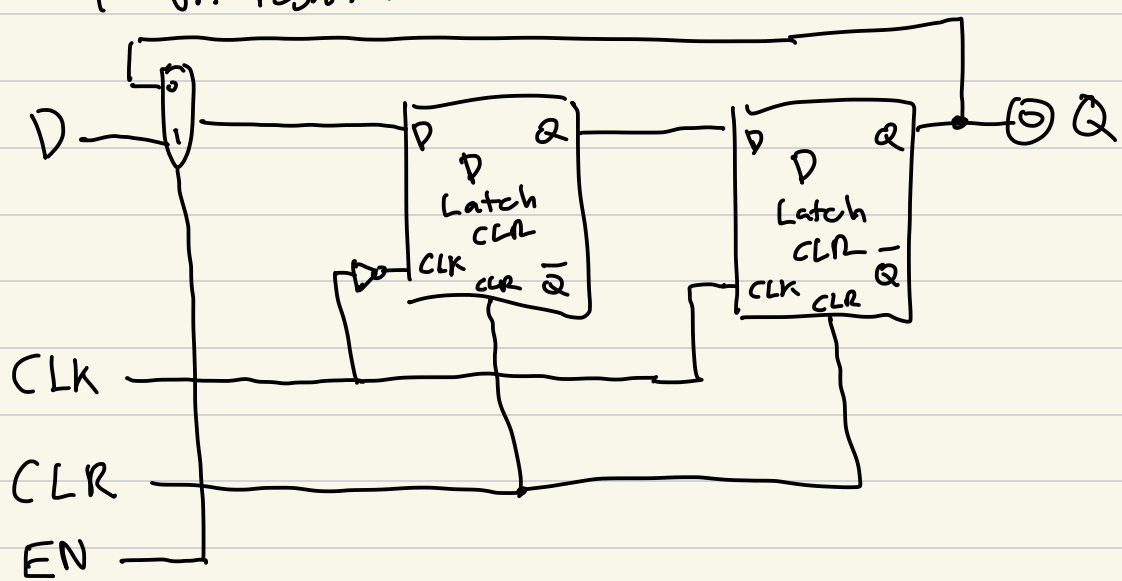


1 bit resister

D Latch with CLR



1 bit resister



4 bit Register